

# CubeSat Subsystem Interface Definition

CSID (Proposal)

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Change Log

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			extension

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## 2 Introduction

The success of the CubeSats was based on standardization of geometric dimensions, allowing joint use of launcher adaptors. An important next step in order to be able to exchange boards at subsystem level would be a specification and standardization of the electrical interfaces, which is addressed in this contribution. There have been attempts in this direction, nevertheless the sometimes used PC104-approach was designed for completely different applications and is not very suitable and efficient for the CubeSat context. With the goal to promote a generic satellite platform related standardized electrical interfaces were realized at the UWE-3 mission, which accumulates in-flight experiences since November 2013. In order to be expanded to a suitable CubeSat standard related interface definitions are summarized in this contribution. The design has been optimized with respect to mass, size and energy efficiency while trying to maintain a modular and flexible architecture. Thus, the proposed bus supports robust and rapid development, integration and testing of the satellite as well as simple maintenance, extension and replacement of subsystems in any configuration during flat-sat development or flight model integration.



Figure 2.1: Overview of the modular UWE-3 pico-satellite bus being optimized for rapid integration and testing and acts as a first reference implementation of the UNISEC bus.

## 3 Mechanical Interface Definition

A standardized backplane (BP+FAB) implements the entire harnessing. Subsystem boards and satellite side panels can be plugged to the backplanes subsystem bus interface and panel bus interface. The resulting electrical structure is fully functional, independent of any further structural component.



Figure 3.1: Backplane Concept for Subsystem Interconnection. FAB and BP (left), partially connected side panels (right).

The backplane implements a redundant set of deployment switches (kill switches) according to CDS<sup>1</sup> 2.3.2 while the front access board implements a backplane extension to provide umbilical line connectors (CDS 2.3.3) and redundant remove-before-flight switches (CDS 2.3.4). The umbilical line is divided in an analog interface for test activation and battery maintenance and a digital interface for software flashing, test and in-system debugging of the onboard computer.

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<sup>&</sup>lt;sup>1</sup> CubeSat Design Specification, The CubeSat Design Program, Rev. 12, Cal Poly SLO



Figure 3.2: Subsystem layout and connector alignment [mm].

The mechanical layout of the backplane is typically adapted to the specific satellite configuration in order to allow desired spatial distribution and especially very compact placement of the subsystems inside the satellite. The electrical bus definition combines the power bus and the data bus and is described in chapter 4.

## 4 Electrical Interface Definition

The electrical interface consists of the standardized debug & maintenance bus, the power bus and the data bus combined on a compact backplane connector. Additionally, a standardized external debug interface can be used for simple stand-alone operation during development, test, and integration.

#### **External Debug Interface**

- easy stand-alone operation of subsystem
- debug communication (UART via USB bridge)
- microcontroller
   programming and insystem-debugging (JTAG, SBW, SWD)
- supply by USB power (5V, 3.3V, unregulated bus)

#### Satellite Bus Connector

- compact and robust backplane
  redundant power, high-speed
- and low-speed digital buses
  dedicated signals for reset, time
- dedicated signals for reset, time sync, deployment logic
- internal debug interface (communication, programming, and debugging after integration and in-orbit)



#### **Power Control Circuit**

- controlled by OBC via redundant I<sup>2</sup>C bus
- power switch
- power monitoring (voltage, current)
- power protection optimized for specific subsystem (over-voltage, under-voltage, overcurrent, i.e. latchup)

#### Interface Control Circuit

- selective bus isolation
   prevents current leakage for
- partial power down
- allows bus routing, redundancy selection controlled by OBC

## 4.1 Debug and Maintenance Bus

#### 4.1.1 Signal Description

Debug & Maintenance	
UML_UART (RXD)	Serial interface for test and debug purpose during development,
UML_UART (TXD)	integration, test and checkout. Inactive in flight mode. Available on the
	digital interface of the umbilical line for checkout tests after integration in
	launch adapter.
UML_SBW-1 (TCK)	General Programming and In-System Debugging interface. Can be used as
UML_SBW-1 (TDIO)	single JTAG interface or redundant Spy-by-Wire (SBW) or Serial Wire
UML_SBW-2 (TCK)	Debug (SWD) interface. Available on the digital interface of the umbilical
UML_SBW-2 (TDIO)	line for software updates after integration in launch adapter.

#### 4.2 Power Bus

The electrical power system (EPS) foresees complete redundant power paths for generation, storage, and conversion. The EPS bases on a peak power tracking architecture with unregulated battery bus implemented in a distributed manner. The power generation block of the EPS is located on the satellite side panels which are connected to the panel bus in order to supply the unregulated battery bus. The power storage block is located on a dedicated subsystem attached to the subsystem bus. A master low side switch allows for global deactivation of all electrical components in order to comply with CDS 2.3.1, 2.3.2, 2.3.2.1, and 2.3.4.2.



Figure 4.1: Distributed Electrical Power Concept.

Besides the unregulated battery bus also 3.3 V and 5 V power lines are available to the subsystems to be able to supply most common types of electrical components. The power buses are distributed to the subsystems via shared power lines on the backplane, while individual power switches with monitoring and protection circuits are directly located on the individual subsystem modules. This topology reduces the number of power lines required on the backplane and ensures that the power distribution capabilities scale with the number of subsystems, being always optimized to their individual requirements.

A standardized interface circuit, the so-called subsystem interface controller (SIC) is implemented on each subsystem of the satellite. Please contact UNISEC-Europe Office to obtain an electrical reference design.



Figure 4.2: Subsystem Interface Control Circuit.

In order to ensure that a subsystem can be completely powered down while other subsystems connected to the backplane are still operating on shared data lines, the subsystem interface controller foresees electrical isolators for each relevant data signal used on a subsystem. Robust analogue switches with overvoltage and power-off protection guarantee that all data lines are high impedance when no power is supplied to the subsystem. Thus, it is ensured that no parasitic current paths, e.g. via standard CMOS ESD protection diodes, prevent the circuit from properly powering down or even cause permanent damage to the device.

# 4.2.1 Signal Description

System Ground and Global Shutdown Control			
GND_SYSTEM	Global ground potential to be used by subsystems. Signal is floating		
	during storage and launch.		
SHDN_CTL-1	Separate shutdown control signals for redundant power paths. Signals		
SHDN_CTL-2	driven by <i>Remove Before Flight Pin</i> and <i>Kill Switch</i> circitury accroding to		
	CDS 2.3.2 and 2.3.4. Affects SUP_3V3, SUP_5V0, SUP_UNREG, and		
	SUP_BACKUP.		

Power Path Source	
PWR_BAT-1	Direct access to redundant unregulated power buses for battery
PWR_BAT-2	maintenance via umbilical line. Can be directly supplied by distributed
	peak power tracker on side panels.
PWR_SC_X	Optional: Input for 3 central independent peak power tracking units. To
PWR_SC_Y	be supplied by the solar panels.
PWR_SC_Z	

Power Supply Buses	
SUP_3V3	3.3V common regulated bus combining both redundant power paths.
SUP_5V0	5.0V common regulated bus combining both redundant power paths.
SUP_UNREG	Common unregulated bus combining both redundant power paths.
SUP_AUX	Common auxiliary bootstrap voltage. Can be supplied by individual bootstrap voltage sources such as solar cells, batteries, etc. Any source should be decoupled by a diode and a current limiting resistor. As SUP_AUX only acts as bootstrap voltage to properly define electrical potentials during hardware bootstrap (e.g. start-up phase from completely depleted batteries), it must NOT be used as power supply for significant loads.
SUP_BACKUP	Common unregulated bus (backup) combining both redundant power paths. Bus bypasses master switches of redundant power paths and is not affected during intentional power cycles initiated by asserting SUP_CTL-1 and SUP_CTL-1 simultaneously.
SUP_CTL-1	Redundant watchdog supervised digital control signals for individual
SUP_CTL-2	deactivation of redundant power paths for maintenance or power cycles. Periodic signal change deactivates corresponding paths contributing to SUP_3V3, SUP_5V0, and SUP_UNREG. Simultaneous assertion initiates power cycle. For power path switch over simultaneous path activation has to be assured during transition. To be controlled by the OBC.

#### 4.3 Data Bus

The data bus provides various signal lines for general subsystem control and communication such as redundant bidirectional communication buses, a subsystem programming interface, global reset and time synchronization. Crucial subsystems such as radio communication and electrical power have dedicated control and communication lines. Further dedicated signal lines allow OBC programming, in-system-debugging, test and checkout after integration via the satellites umbilical line.

General Subsystem Control			
BUS_I2C-1 (SDA)	Redundant I <sup>2</sup> C interfaces for bidirectional low-rate data exchange among		
BUS_I2C-1 (SCL)	subsystems or direct access to remote I <sup>2</sup> C devices (i.e. power monitors,		
BUS_I2C-2 (SDA)	temperature sensors). Subsystems might use the buses in multi-master		
BUS_I2C-2 (SCL)	mode for reception (subsystem is slave as default) and transmission		
	(subsystem becomes master when required).		
BUS_MLVDS-1 (D+)	Redundant Multi-Point LVDS interface for bidirectional high-speed data		
BUS_MLVDS-1 (D-)	exchange among subsystems. Each data bus consists of a differential		
BUS_MLVDS-1 (C+)	synchronous serial interface including data line (D+/D-) and clock line		
BUS_MLVDS-1 (C-)	(D+/D-) and might be driven by any subsystem depending on bus		
BUS_MLVDS-2 (D+)	arbitration technique used by upper protocol layers.		
BUS_MLVDS-2 (D-)			
BUS_MLVDS-2 (C+)			
BUS_MLVDS-2 (C-)			
CTL_RESET	Global not-reset signal (low-active) driven by the OBC (default high).		
CTL_SYNC	Global synchronization signal, driven by the OBC.		
GPIO	General Purpose Input/Output Line		

## 4.3.1 Signal Description

Special Subsystem Control: Communication			
COM_UART-1 (RXD)	Redundant serial interfaces for dedicated one-2-one communication with		
COM_UART-1 (TXD)	the redundant radio communication subsystem.		
COM_UART-2 (RXD)			
COM_UART-2 (TXD)			
COM_IRQ	Dedicated interrupt request from redundant radio communication		
	subsystem to indicate incoming frame.		

# 4.4 Unified Subsystem Connector

# 4.4.1 Connector Types

Subsystem Connector		Backplane Connector		
CSID_SUB_RA	CSID_SUB_ST	CSID_BP_RA	CSID_BP_ST	
			Communication of the second	
ERNI MicroCon 0.8mm	ERNI MicroCon 0.8mm	ERNI MicroCon 0.8mm	ERNI MicroCon 0.8mm	
www.erni.com	www.erni.com	www.erni.com	www.erni.com	
50 pin	50 pin	50 pin	50 pin	
female	female	male	male	
RA	ST	RA	ST	
294257	294006	294288	294139	

# 4.4.2 Example Configuration in a compact 1U spacecraft



The following sections define the connector and pin layout of the individual interfaces.

## 4.4.3 Signal Layout

Debug & Maintenance Bus	Data Bus		Power Bus
UML_UART (RXD)	1	2	UML_UART (TXD)
UML_SBW-1 (TDIO/TDO)	3	4	UML_SBW-1 (TCK/TCK)
UML_SBW-2 (TDIO/TMS)	5	6	UML_SBW-2 (TCK/TDI)
BUS_I2C-1 (SDA)	7	8	BUS_I2C-1 (SCL)
BUS_MLVDS-1 (D+)	9	10	BUS_MLVDS-1 (C+)
BUS_MLVDS-1 (D-)	11	12	BUS_MLVDS-1 (C-)
GND_SYSTEM	13	14	GND_SYSTEM
SUP_5V0	15	16	SUP_5V0
CTL_RESET	17	18	CTL_RESET
COM_UART-1 (RXD)	19	20	BUS_I2C-2 (SDA)
COM_UART-1 (TXD)	21	22	BUS_I2C-2 (SCL)
SUP_UNREG	23	24	SUP_UNREG
SUP_3V3	25	26	SUP_3V3
PWR_BAT-2	27	28	PWR_BAT-2
PWR_BAT-1	29	30	PWR_BAT-1
reserved (PWR_SC_Y)	31	32	reserved (PWR_SC_X)
reserved (PWR_SC_Z)	33	34	CTL_SYNC
GND_SYSTEM	35	36	GND_SYSTEM
SHDN_CTL-1	37	38	SHDN_CTL-2
SUP_AUX	39	40	SUP_BACKUP
SUP_CTL-1	41	42	SUP_CTL-2
BUS_MLVDS-1 (D+)	43	44	BUS_MLVDS-1 (C+)
BUS_MLVDS-1 (D-)	45	46	BUS_MLVDS-1 (C-)
COM_UART-2 (TXD)	47	48	COM_IRQ
COM_UART-2 (RXD)	49	50	General Purpose Input/Output

### **5** Conclusions

This document outlines an efficient electrical interface standard for CubeSats (including maintenance, data and power bus), exhibiting the potential for increased exchange at subsystem board level within the CubeSat community.

#### 6 Contact

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